

IN THE CLAIMS

Unchanged claim 1

1 1. An active inductor for use on an integrated circuit having a power supply
2 voltage supplied from a first power supply terminal, comprising:

3 an metal oxide semiconductor (MOS) transistor having a gate terminal, a drain
4 terminal, and a source terminal, said drain terminal being coupled to said power supply
5 voltage and said source terminal being one of the terminals of said active inductor; and

6 a resistor having a first terminal coupled to said gate terminal and a second
7 terminal coupled to a voltage that is derived from said power supply voltage and has a
8 larger absolute value than said power supply voltage supplied by said first power supply
9 terminal and the same sign as said power supply voltage.

Amend claim 2

~~1 2~~ ~~Sub 2~~ 2. (Amended) The invention as defined in claim 1 wherein [said] the other one of
the terminals of said active inductor is said first power supply terminal.

Unchanged claim 3

1 3. The invention as defined in claim 1 wherein said MOS transistor also has a
2 bulk terminal, said bulk terminal being connected to a second power supply terminal.

Amend claim 4

~~1~~ ~~2~~ 4. (Amended) The invention as defined in claim 1 wherein MOS transistor is a
negative metal oxide semiconductor (NMOS) transistor.

Amend claim 5

1 5. (Amended) The invention as defined in claim 1 wherein MOS transistor is a
2 positive metal oxide semiconductor (PMOS) transistor.

Unchanged claim 6

1 6. The invention as defined in claim 1 wherein said MOS transistor also has a
2 bulk terminal, said bulk terminal being connected to a second power supply terminal, and
3 wherein said power supply voltage supplied from said first power supply terminal is
4 higher than a voltage supplied from said second power supply terminal.

Unchanged claim 7

1 7. The invention as defined in claim 1 wherein said MOS transistor also has a
2 bulk terminal, said bulk terminal being connected to a second power supply terminal, and
3 wherein said power supply voltage supplied from said first power supply terminal is
4 lower than a voltage supplied from said second power supply terminal.

Amend claim 8

1 8. (Amended) The invention as defined in claim 1 wherein said MOS transistor is
2 a negative metal oxide semiconductor (NMOS) transistor, said NMOS transistor also has
3 a bulk terminal, said bulk terminal being connected to a second power supply terminal,
4 and wherein said first power supply terminal is the positive power supply terminal for
5 said integrated circuit and said second power supply terminal is the negative power
6 supply terminal for said integrated circuit.

[Amend claim 9]

1 9. (Amended) The invention as defined in claim 1 wherein said MOS transistor is
2 a positive metal oxide semiconductor (PMOS) transistor, said PMOS transistor also has a
3 bulk terminal, said bulk terminal being connected to a second power supply terminal, and
4 wherein said first power supply terminal is the negative power supply terminal for said
5 integrated circuit and said second power supply terminal is the positive power supply
6 terminal for said integrated circuit.

Unchanged claim 10

1 10. The invention as defined in claim 1 wherein said voltage that is derived from
2 said power supply voltage and has a larger absolute value than said power supply voltage
3 supplied by said first power supply terminal and the same sign as said power supply
4 voltage has a larger absolute value than said power supply by one threshold voltage of
5 said MOS transistor.

Unchanged claim 11

1 11. The invention as defined in claim 1 wherein said voltage that is derived from
2 said power supply voltage is generated from said power supply voltage by a high voltage
3 generator.

Unchanged claim 12

1 12. The invention as defined in claim 1 further including on said integrated
2 circuit a high voltage generator that generates said voltage that has a larger absolute value
3 than said power supply voltage supplied by said first power supply terminal and the same
4 sign as said power supply voltage.

Unchanged claim 13

1 13. The invention as defined in claim 1 further including on said integrated
2 circuit a high voltage generator that generates said voltage that has a larger absolute value
3 than said power supply voltage supplied by said first power supply terminal and the same
4 sign as said power supply voltage, said high voltage generator comprising:

5 an oscillator generating an oscillating output signal;

6 a voltage doubler receiving as an input said oscillating output signal from said
7 oscillator and supplying as an output a signal that has an average larger absolute value
8 than said power supply voltage supplied by said first power supply terminal and the same
9 sign as said power supply voltage;

10 a clamp which receives as an input said output of said voltage doubler and
11 supplies an output voltage substantially clamped to a prescribed value that has a larger
12 absolute value than said power supply voltage supplied by said first power supply
13 terminal and the same sign as said power supply voltage;

14 and a ripple filter which filters said output of said clamp and supplies the output
15 of said high voltage generator, which said voltage that has a larger absolute value than
16 said power supply voltage supplied by said first power supply terminal and the same sign
17 as said power supply voltage.

Unchanged claim 14

1 14. An active inductor on an integrated circuit, comprising:
2 a metal oxide semiconductor (MOS) transistor; and *a predecessor*
3 a high voltage generator which generates a voltage outside the range of voltages
4 being supplied to said integrated circuit by a power supply;
5 wherein said MOS transistor is coupled to said high voltage generator so as to
6 bias said MOS transistor with said voltage outside the range of voltages being supplied to
7 said integrated circuit by a power supply.

Unchanged claim 15

1 15. The invention as defined in claim 14 wherein said high voltage generator
2 comprises:
3 an oscillator generating an oscillating output signal;
4 a voltage doubler receiving as an input said oscillating output signal from said
5 oscillator and supplying as an output a voltage signal that has an average voltage that is
6 outside the range of voltages being supplied to said integrated circuit by a power supply;
7 a clamp which receives as an input said output of said voltage doubler and
8 supplies an output voltage substantially clamped to a prescribed value that is outside the
9 range of voltages being supplied to said integrated circuit by a power supply;
10 and a ripple filter which filters said output of said clamp and supplies the output
11 of said high voltage generator.

Unchanged claim 16

1 16. An active inductor on an integrated circuit, said active inductor comprising a
2 metal oxide semiconductor (MOS) transistor and being characterized in that said active
3 inductor is biased using a voltage generated on said integrated circuit that is beyond the
4 range of the voltage supplied by a power supply for operating said integrated circuit.

Amend claim 17

AM
1 17. (Amended) The invention as defined in claim 16 wherein said MOS transistor
2 is a negative metal oxide semiconductor (NMOS) transistor.

Amend claim 18

1 18. (Amended) The invention as defined in claim 16 wherein said MOS transistor
2 is a positive metal oxide semiconductor (PMOS) transistor.

Unchanged claim 19

19. The invention as defined in claim 16 wherein said active inductor is biased by
coupling a gate of said MOS transistor to said voltage generated on said integrated circuit
that is beyond the range of the voltage supplied by a power supply for operating said
integrated circuit via an impedance.